Customer No. 22,852
Attorney Docket No.: **04329.3138**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Kouji MATSUO	)	
	)	Group Art Unit: **Not Yet Assigned**
Serial No.: **Not Yet Assigned**	)	
	)	Examiner: **Not Yet Assigned**
Filed: **September 12, 2003**	)	
	)	
For: **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**	)	

MAIL STOP PATENT APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicant brings to the Examiner's attention the documents listed on attached Form PTO-1449. With exception of the U.S. patents, copies of the listed documents are attached. Applicant respectfully requests that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form. This Information Disclosure Statement is being filed with the above-referenced application.

The following is a concise statement of relevance of the non-English language documents:

1. Japanese Patent Publication No. 2000-195966 – discloses a part of logic transistors are polysilicon gate and other logic transistors are metal gate (Fig. 3b).

2. Japanese Patent Publication No. 2002-270797 - discloses DRAM and part of logic transistors are recessed channel transistors (Fig. 22).

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3. Japanese Patent Publication No. 2002-530864 - discloses transistor shape similar to recessed channel transistor (Fig. 6).

Also, an English-language abstract of documents 1 and 2 above is enclosed.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicant determines that the cited documents do not constitute "prior art" under United States law, applicant reserves the right to present to the office the relevant facts and law regarding the appropriate status of such documents. Applicant further reserves the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
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Dated: September 12, 2003

By: _____
Richard V. Burgujian
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Enclosures
RVB/FPD/sci

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INFORMATION DISCLOSURE CITATION

Atty. Docket No.	**04329.3138**	Serial No.	**Not Yet Assign d**
Applicant	**Kouji MATSUO**		
Filing Date	**September 12, 2003**	Group:	**Not Yet Assigned**

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		6,376,888	04/23/02	**TSUNASHIMA** et al.			
		2003-0143825 A1	07/31/03	**MATSUO** et al.			

FOREIGN PATENT DOCUMENTS

		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
		2000-195966	07/14/00	JAPAN			ABSTRACT
		2002-270797	09/20/02	JAPAN			ABSTRACT
		2002-530864	09/17/02	JAPAN			NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	MATSUO, K., "Semiconductor Device and Method of Manufacturing the Same", U.S. Application No. 10/396,453, filed March 26, 2003.

Examiner	Date Considered
*Examiner:	Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce